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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kevin Frazier, et al.
Serial No: Herewith
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For: MULTI-PROTOCOL PACKET TRANSLATOR

Examiner: Not Assigned
Art Unit: Not Assigned

BOX PATENT APPLICATION
COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

Sir:

**PRELIMINARY AMENDMENT**

In the Specification

Page 5, line 12, after "While" insert --the--

Page 7, line 12, after "(MPT)" insert --26--

Page 11, line 8, after "processing." insert — Addressing of the dump memory 57 may be controlled by an address control unit 57a.--

Page 16, line 2, after "FIG. 5" insert --STEP 85--

Page 16, line 7, after "translation" insert --88--

Page 25, line 18, after "stage" insert --112--

Page 25, line 18, after "instruction" insert --112a-112d--

Page 26, line 11, after "stage" insert --112--

Page 28, line 18, after "written" insert --155--

In the Claims

Please add the following new claims 22-33:

22. A pipelined control unit for controlling pipelined translations between a first data packet having a first protocol and a second data packet having a second protocol, comprising:

a pipeline unit having at least a first stage and a second stage;

an input memory having a first latency and storing the first data packet;

an information source having a second latency and storing translation information to translate the first data packet into the second data packet; and

a control circuit coupled to the pipeline unit which causes the input memory to begin a read cycle during the first stage and which causes the information source to begin a read cycle during the second stage.

23. The system of claim 24, wherein the information contained in the information source is new header information used to translate from the first protocol to the second protocol.

24. The system of claim 25, wherein a first register of the pipeline unit contains opcodes and the a second register contains operands.

25. The system of claim 26, wherein the opcodes in the first register are used to determine whether information from the input memory or the information source or the pipeline unit should used to perform the translation.

26. The system of claim 24, wherein the pipeline unit is a double pipeline unit having two three-stage pipelines.

27. A pipelined control unit for reading data comprising:

a first memory having a first latency;

a second memory having a second latency;

a pipeline unit having a first set of registers for processing an operand and a second set of registers for processing an opcode, the pipeline unit having a first stage and a second stage; and

a control circuit coupled to the first memory, the second memory, and the pipeline unit for initiating a read cycle in the first memory during the first stage and for initiating a read cycle in the second memory during the second stage.

28. The pipelined control unit of claim 29, wherein the first set of registers includes three 8-bit registers.

29. The pipelined control unit of claim 29, wherein the second set of registers includes three 8-bit registers.

30. The pipelined control unit of claim 29, wherein the pipeline unit is a double pipeline unit.

31. The pipelined control unit of claim 32, wherein the double pipeline unit includes two channels, each channel being 16 bits wide.

32. The pipelined control unit of claim 29, wherein the pipeline unit is a quad pipeline unit.

33. The pipelined control unit of claim 29, further comprising a microcontroller coupled to the control circuit.

**REMARKS**

Each of the new claims is fully supported by the specification and no new matter has been added.

Respectfully Submitted,

Matthew B. Lowrie,, Reg. No. 38,228
M. Brad Lawrence, Reg. No. 47210
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, MA 02210-2211
(617) 720-3500

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